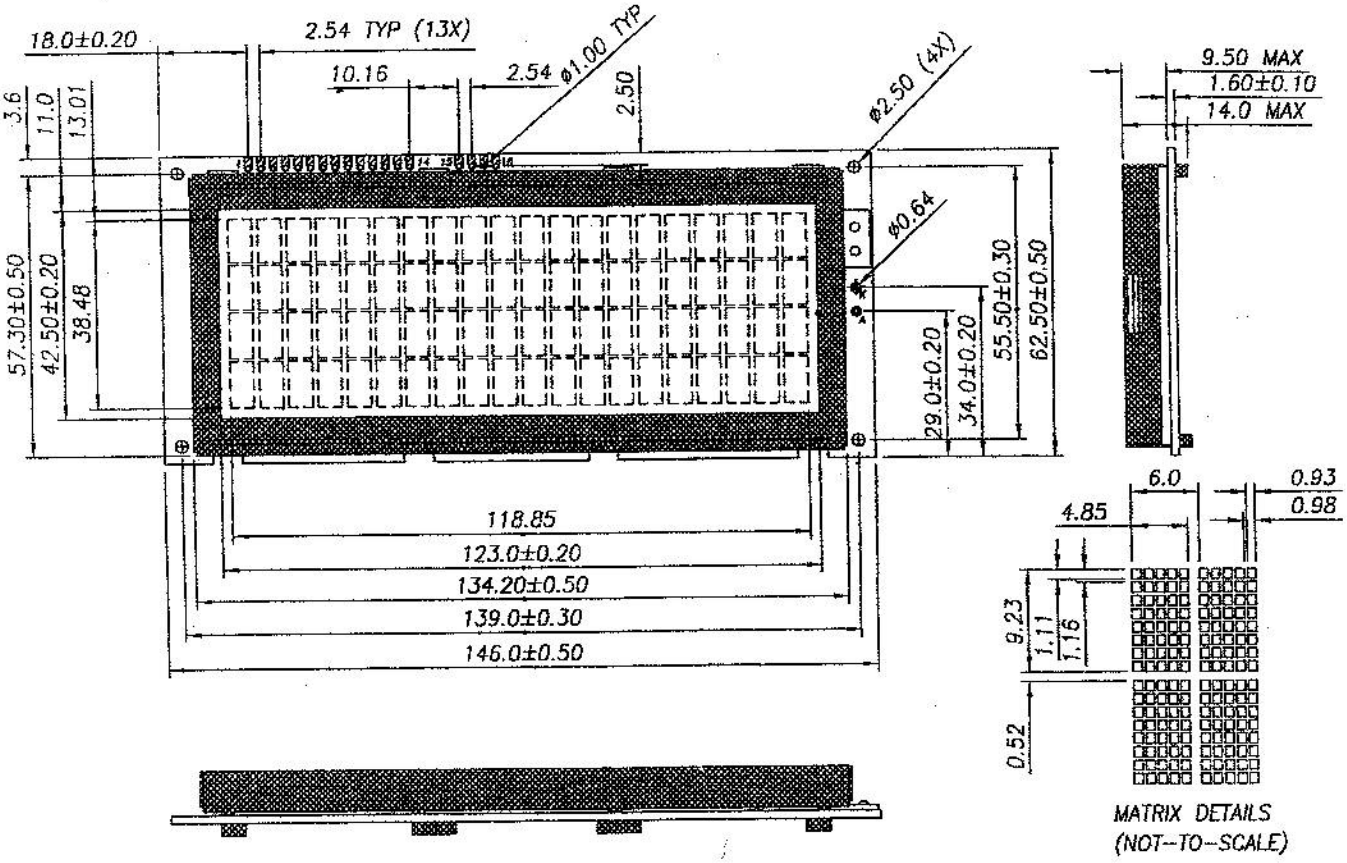
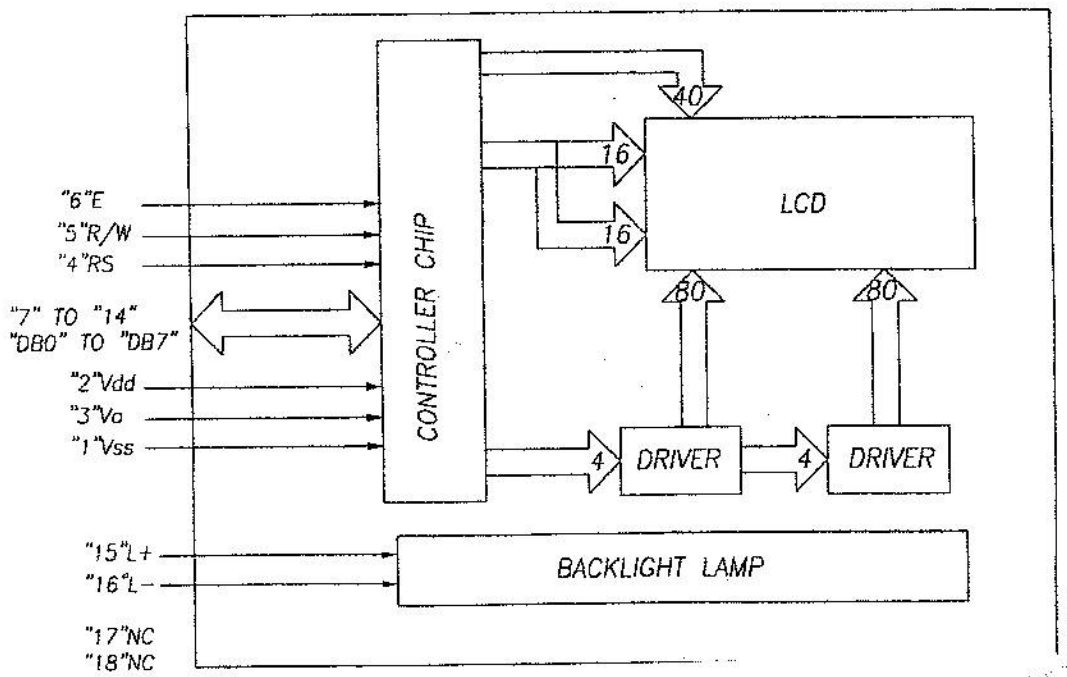
SPECIFICATIONS FOR ALPHANUMERIC DOT MATRIX MODULES



Block Diagram



HITECH DISPLAYS SDN BHD

DOT MATRIX MODULES

DEFINITION OF TERMINALS

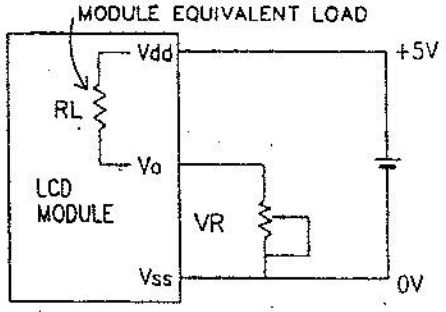
PIN NO.	SYMBOL	FUNCTION
1	V_{SS}	Ground terminal of module
2	V_{DD}	Supply terminal of module, +5V
3	Vo	Power supply for Liquid crystal Drive
4	RS	Register Select RS = 0 ... Instruction Register RS = 1 ... Data Register
5	R/W	Read/Write R/W = 1 ... Read R/W = 0 ... Write
6	E	Enable
7–14	DB0–DB7	Bi-directional Data Bus. Data Tranfer is performed once, thru DB0–DB7, in the case of interface data length is 8-bits; and twice, thru DB4–DB7, in the case of interface data length is 4-bits. Upper four bits first then lower four bits.
15 16	L– L+	LED or EL lamp power supply terminals

OPERATING SPECIFICATIONS

	STANDARD TEMP	WIDE TEMP
Operating temperature range	0°C to +50°C	−20°C to +70°C
Storage temperature range	−10°C to +60°C	−30°C to +75°C
Operating relative humidity	90% MAX	90% MAX

POWER SUPPLY REQUIREMENTS

- Wide Temperature Range Version
- Standard
- Super-Twist Display Version



When RL=23.5K, VR=10~20K
RL=5K, VR=2~5K

This circuit shows the typical power supply connection for all dot matrix module. The display Voltage (V_{LCD}) is slightly different for different version (eg. standard, wide temp and supertwist.) Recommend end user to use VARIABLE RESISTOR as shows in the circuit for optimum V_{LCD} ($V_{DD}-V_O$) adjustment to obtain best display contrast and viewing angle.

ELECTRICAL CHARACTERISTICS (To = +25°C)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
LCD Drive Voltage Normal Temp Model (TN/STN) Wide Temp Model (STN)	$V_{DD}-V_O$ (V_{LCD})		 4.2 6.4	 4.5 6.8	 4.8 7.5	 V V
Supply Current[1] 1 x 16 DMM 2 x 16 DMM 1 x 20, 2 x 20, 2 x 24 DMM 4 x 20, 2 x 40 DMM	I_{DD}	V_{DD} = 5V V_O = 0V MIN	 – – – –	 1.0 1.0 1.5 2.5	 2.0 3.0 3.0 4.0	 mA mA mA mA
Input Voltage[2]	V_{IL} V_{IH}		0 2.0	– –	0.6 V_{DD}	V V
Output Voltage[3]	V_{OL} V_{OH}	I_{OL} = 1.6mA I_{OH} = 0.2mA	– 2.4	– –	0.4 –	V V
LED Current 1 x 16, 2 x 16 DMM 2 x 24, 2 x 20 DMM 1 x 20, 1 x 40, 2 x 40, 4 x 20 DMM	I_{LED}	L+ – L– = 5V	 – – –	 40 60 150	 60 80 250	 mA mA mA

DRIVE VOLTAGE(V_{LCD}) IS NOT IDENTICAL FOR LCD MODULES MANUFACTURES. ACCEPTABLE RESULTS CAN BE OBTAINED BY ADJUSTING V_{LCD}. IF THIS DOES NOT WORK, HITECH CAN MODIFY DISPLAY TO MEET CUSTOM NEEDS.

Note: 1. Applies to DB0 – DB7, E, RS and R/W
2. Applies to DB0 – DB7
3. Supply current may slightly exceed MAX. Rating if SAMSUNG controller is used. without pull-up resistor for DB0 – DB7.

HITECH DISPLAYS SDN BHD

DOT MATRIX MODULES

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INSTRUCTION SET

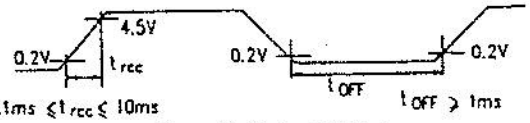
INSTRUCTION	CODE										DESCRIPTION	TYPICAL EXECUTION TIME
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	0	0	0	0	0	0	0	0	0	1	Clears display and returns the cursor to home position (Address 0). Sets I/D=1 of Entry Mode.	1.64 ms
Return home	0	0	0	0	0	0	0	0	1	●	Return the cursor to the home position (Address 0). Also returns the display being shifted to the original position. DD RAM contents remain unchanged. Set DD RAM addresses to zero.	1.64 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Set the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read of DD RAM/CG RAM. FOR NORMAL OPERATION, SET S TO 0	40 μs
Display ON/Off control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF all display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40 μs
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	●	●	Moves the cursor and shifts the display without changing DD RAM contents.	40 μs
Function set	0	0	0	0	1	DL	N	F	●	●	Sets interface data length (DL) number of display lines (N) and character font (F).	40 μs
Set the CG RAM address	0	0	0	1	MSB ACG					LSB	Sets the CG RAM address. CG RAM data is sent and received after this setting.	40 μs
Set the DD RAM address	0	0	1	MSB ADD						LSB	Sets the DD RAM address. DD RAM data is sent and received after this setting.	40 μs
Read busy flag & address	0	1	BF	MSB AC						LSB	Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	40 μs
Write data to CG or DD RAM	1	0	MSB							LSB	Writes data into DD RAM or CG RAM.	40 μs
Read data from CG or DD RAM	1	1	MSB							LSB	Reads data from DD RAM or CG RAM.	40 μs
	S =1: Accompanies display shift when data is written. for normal operation, set to 0 I/D=1: Increment DL=1 : 8 bits I/D=0: Decrement DL=0 : 4 bits S/C=1: Display shift N =1 : 2 (1) line S/C=0: Cursor move N =0 : 1 line R/L=1: Shift to the right F =1 : 5x10 dots R/L=0: Shift to the left F =0 : 5x7 dots BF =1: Internally operating BF =0: Can accept instruction										DD RAM : Display data RAM CG RAM : Character generator RAM ACG : CG RAM address ADD : DD RAM address corresponds to cursor address AC : Address counter used for both DD and CG RAM address B : 1=ON 0=OFF (Blinking cursor) C : 1=ON 0=OFF (Cursor) D : 1=ON 0=OFF (Display) ●Don't Care	

INITIALIZATION

The module automatically performed initialization when powered on (using internal reset circuit). The following instructions are executed during initialization :-

1. CLEAR DISPLAY
   The Busy Flag is kept in the Busy State (BF=1) until initialization ends. The time is 15 ms.
2. Function Set ---------- DL= 1: 8-bits long interface data
   N = 0 : 1 Line display
3. DISPLAY ON/OFF CONTROL--- D = 0 : Display OFF
   C = 0 : Cursor OFF
   B = 0 : Blink OFF
4. ENTRY MODE SET -------- I/D= 1 : +1(INCREMENT)
   S = 0 : NO SHIFT
5. DD RAM IS SELECTED
   Power On Initialization depends on rise time of the supply when it is turned on. The following time relationship must be satisfied.

ITEM	SYMBOL	STANDARD TIME MIN	TYP	MAX	UNIT
Power Supply Rise Time	t_{rcc}	0.1	-	10	ms
Power Supply Off Time	t_{OFF}	1.0	-	-	ms



0.1ms ≤ t_{rcc} ≤ 10ms t_{OFF} ≥ 1ms

Power On Timing Diagram

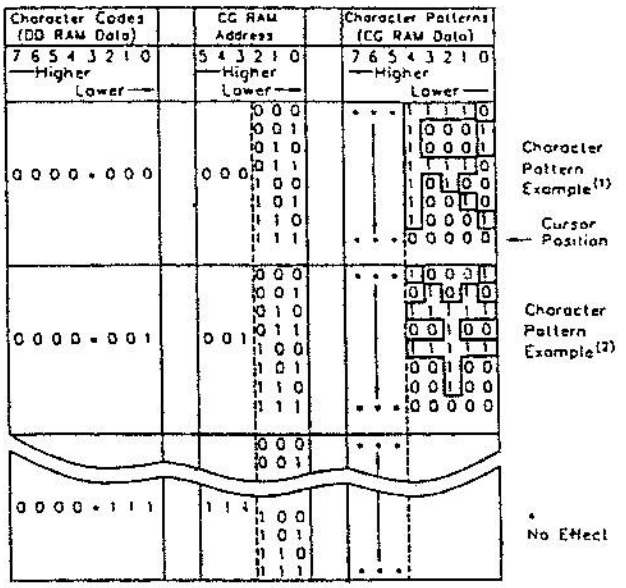
NOTE :
When the above power supply condition is not satisfied, the internal reset circuitry does not operate correctly. In this case, perform the needed initialization by sending function set instructions thrice from MPU after turning the power on. For example, to designate a 8-bits data length, send the following instructions thrice.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	●	●	●	●
0	0	0	0	1	1	●	●	●	●
0	0	0	0	1	1	●	●	●	●

When this ends, the module enters 8-bits data length mode without fail. then enter 4-bits data length instruction for 4-bits data length interface.

DOT CHARACTER PATTERNS

For 5x7 Dot Character Patterns



NOTE:
Character code bits 0,2 correspond to CG RAM address bits 3,5 (3 bits : 8 types)

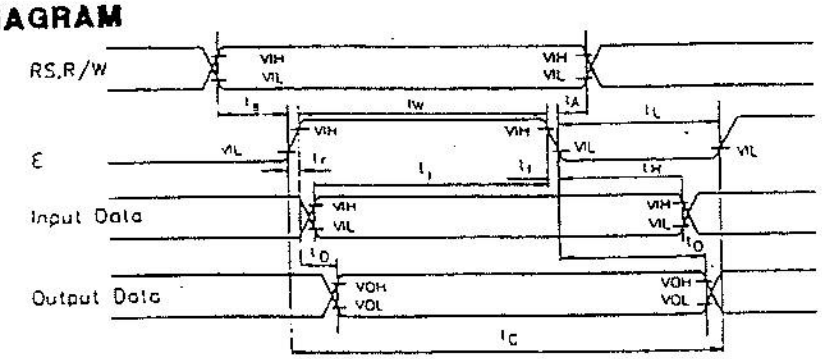
TIMING CHARACTERISTICS FOR CONTROLLER CHIPS.

PARAMETERS \ CONTROLLERS CHIPS		SAMSUNG KS0066	RECOMMENDED TIMING	UNIT
Enable Cycle Time	tC (min)	1000	1000	nS
Enable Pulse Width High Level Low Level	tW (min) tL (min)	450 450	450 450	nS nS
E Raise Time	tr (max)	25	25	nS
E Fall Time	tf (max)	25	25	nS
Set-up Time	tS (min)	140	140	nS
Data Set-up Time	tI (min)	195	195	nS
Data Delay Time	tD (max)	320	320	nS
Address Hold Time	tA (max)	10	10	nS
Hold Time Input Data Output Data	tH (min) tO (min)	10 20	10 20	nS nS

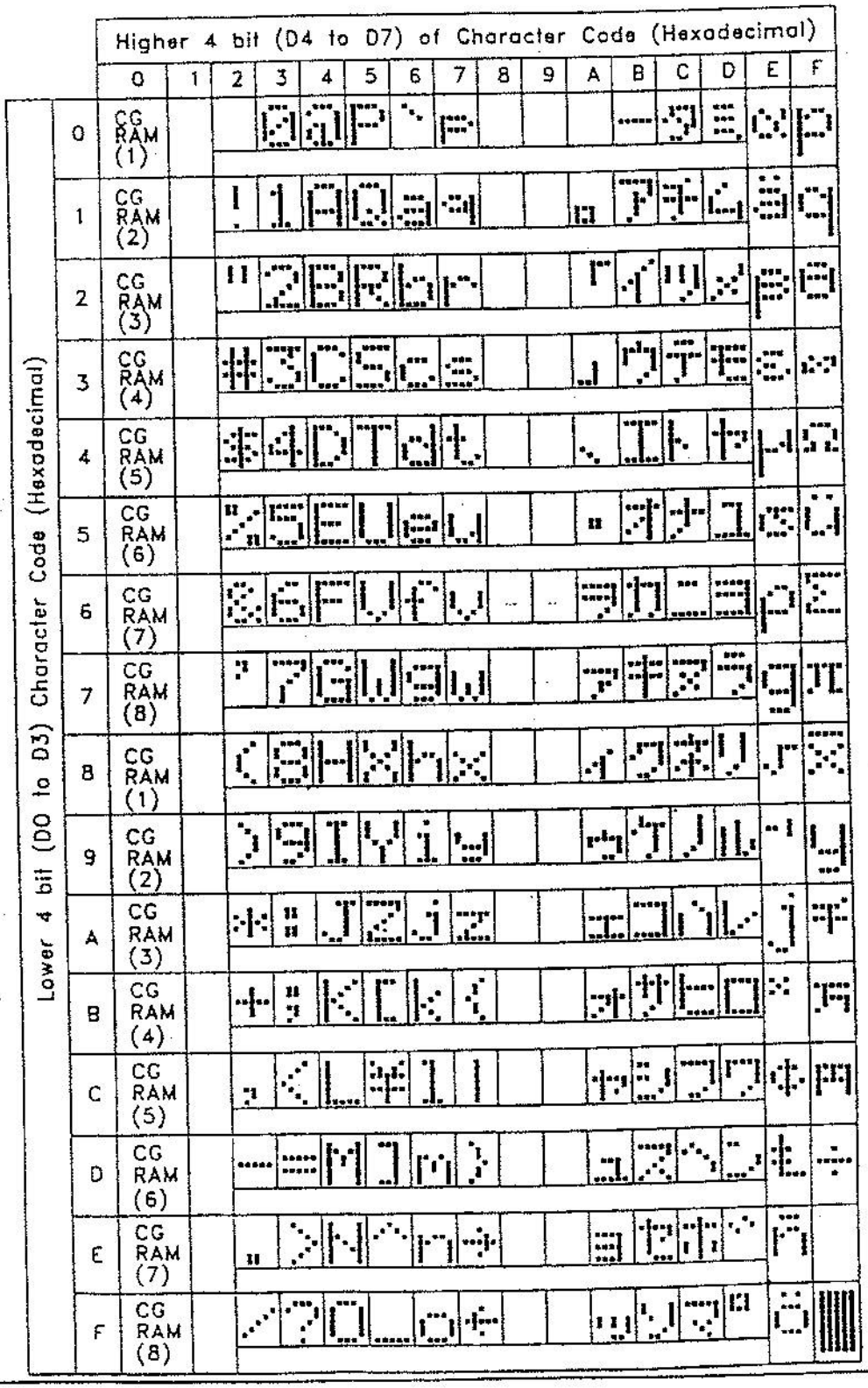
NOTE :

1. INITIALIZATON BY POWER-ON RESET INVOLVES MANY UNSTABLE FACTORS CAUSED BY POWER SUPPLY FLUCTUATIONS. THEREFORE, INITIALISING BY INSTRUCTIONS IS STRONGLY RECOMMEDED.

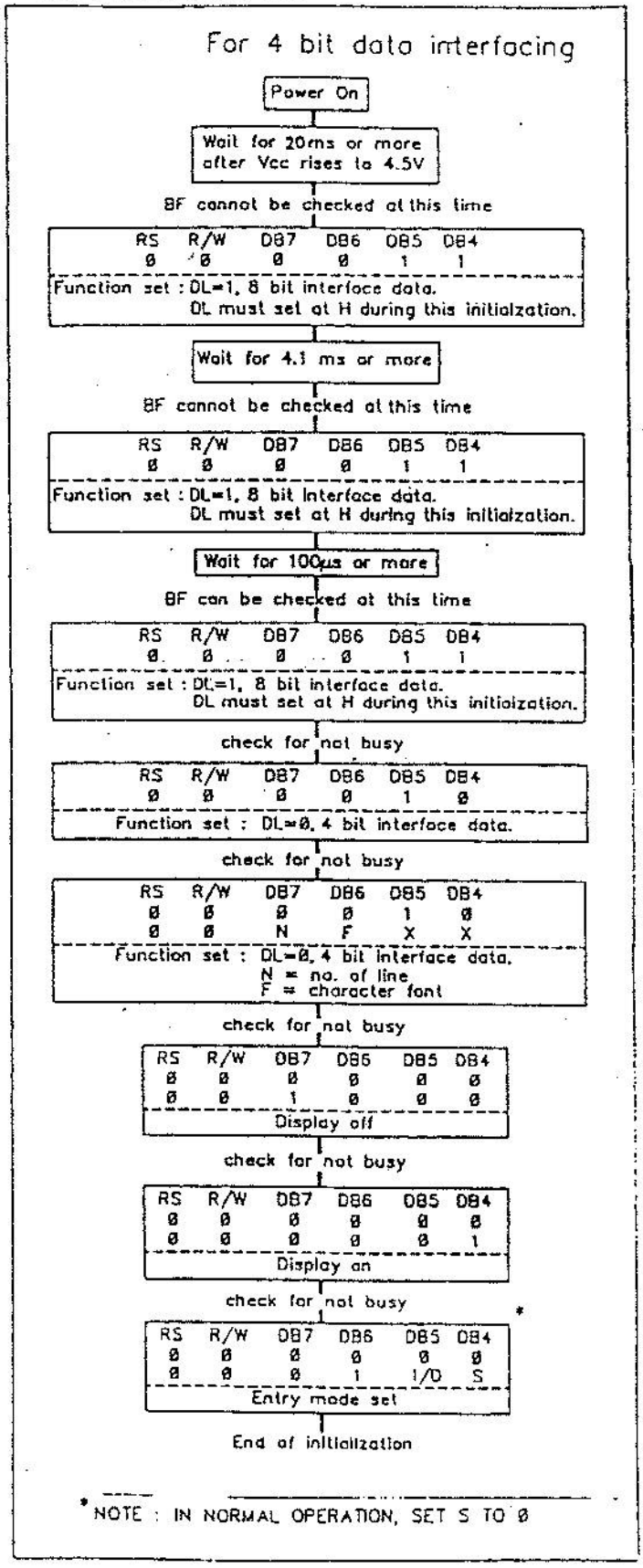
TIMING DIAGRAM



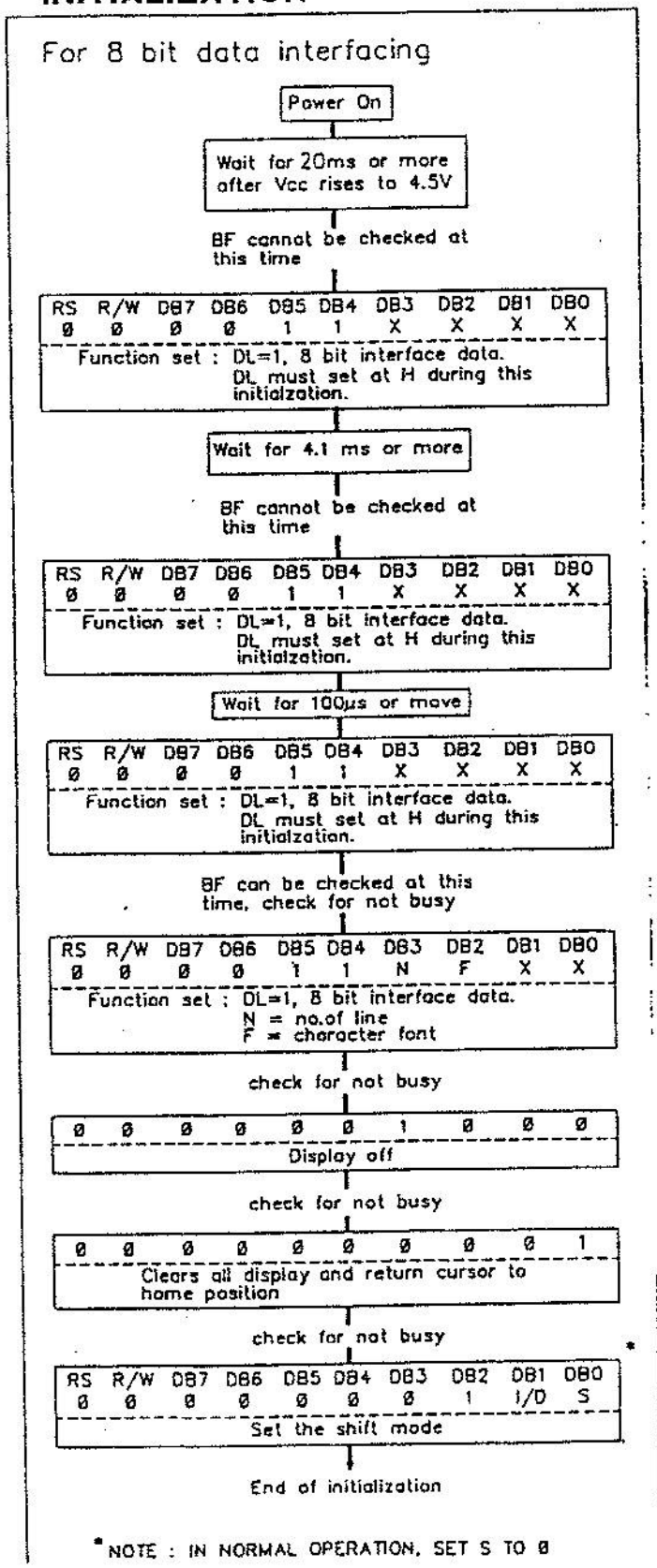
CHARACTER CODE MAP



INITIALIZATION



INITIALIZATION



*NOTE : IN NORMAL OPERATION, SET S TO 0

DISPLAY CHARACTER POSITION AND DD RAM ADDRESS

1x8 DMM, 1/8 MUX

N=0 : 1-LINE DISPLAY
F=0 : 5X7 DOTS

	1	2	3	4	5	6	7	8	
									DISPLAY POSITION
FIRST LINE	00	01	02	03	04	05	06	07	DD RAM ADDRESS

WHEN THE DISPLAY SHIFT OPERATION IS PERFORMED, THE DD RAM ADDRESS MOVED AS FOLLOW :

AFTER THE LEFT SHIFT INSTRUCTION

1	2	3	4	5	6	7	8	
								DISPLAY POSITION
01	02	03	04	05	06	07	08	DD RAM ADDRESS

AFTER THE RIGHT SHIFT INSTRUCTION

1	2	3	4	5	6	7	8	
								DISPLAY POSITION
4F	00	01	02	03	04	05	06	DD RAM ADDRESS

1x16 DMM, 1/16 MUX

N=1 : 2-LINE DISPLAY
F=0 : 5X7 DOTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
																	DISPLAY POSITION
FIRST LINE	00	01	02	03	04	05	06	07	40	41	42	43	44	45	46	47	DD RAM ADDRESS

WHEN THE DISPLAY SHIFT OPERATION IS PERFORMED, THE DD RAM ADDRESS MOVED AS FOLLOW :

AFTER THE LEFT SHIFT INSTRUCTION

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
																DISPLAY POSITION
01	02	03	04	05	06	07	08	41	42	43	44	45	46	47	48	DD RAM ADDRESS

AFTER THE RIGHT SHIFT INSTRUCTION

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
																DISPLAY POSITION
27	00	01	02	03	04	05	06	67	40	41	42	43	44	45	46	DD RAM ADDRESS

1x16 DMM, 1/8 MUX

N=0 : 1-LINE DISPLAY
F=0 : 5X7 DOTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
																	DISPLAY POSITION
FIRST LINE	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DD RAM ADDRESS

1x20 DMM, 1/8 MUX

N=0 : 1-LINE DISPLAY
F=0 : 5X7 DOTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
																					DISPLAY POSITION
FIRST LINE	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	DD RAM ADDRESS

1x40 DMM, 1/11 MUX

N=0 : 1-LINE DISPLAY
F=1 : 5X10 DOTS

	1	2	3	4	5	6	7	8	9	10	11	12	13		33	34	35	36	37	38	39	40	
																							DISPLAY POSITION
FIRST LINE	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	---	20	21	22	23	24	25	26	27	DD RAM ADDRESS

DISPLAY CHARACTER POSITION AND DD RAM ADDRESS (CONTINUE)

2x16 DMM, 1/16 MUX N=1 : 2-LINE DISPLAY F=0 : 5X7 DOTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
																	DISPLAY POSITION
FIRST LINE	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DD RAM ADDRESS
SECOND LINE	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

WHEN THE DISPLAY SHIFT OPERATION IS PERFOMED, THE DD RAM ADDRESS MOVED AS FOLLOW :

AFTER THE LEFT SHIFT INSTRUCTION

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
																DISPLAY POSITION
01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	DD RAM ADDRESS
41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	

AFTER THE RIGHT SHIFT INSTRUCTION

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
																DISPLAY POSITION
27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	DD RAM ADDRESS
67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	

2x20 DMM, 1/16 MUX N=1 : 2-LINE DISPLAY F=0 : 5X7 DOTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
																					DISPLAY POSITION
FIRST LINE	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	DD RAM ADDRESS
SECOND LINE	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	

2x24 DMM, 1/16 MUX N=1 : 2-LINE DISPLAY F=0 : 5X7 DOTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	
																									DISPLAY POSITION
FIRST LINE	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	DD RAM ADDRESS
SECOND LINE	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	

2x40 DMM, 1/16 MUX N=1 : 2-LINE DISPLAY F=0 : 5X7 DOTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	...	33	34	35	36	37	38	39	40	
																							DISPLAY POSITION
FIRST LINE	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	-------	20	21	22	23	24	25	26	27	DD RAM ADDRESS
SECOND LINE	40	41	42	43	44	45	46	47	48	49	4A	4B	4C		60	61	62	63	64	65	66	67	

4x16 DMM, 1/16 MUX N=1 : 2-LINE DISPLAY F=0 : 5X7 DOTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
																	DISPLAY POSITION
FIRST LINE	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	DD RAM ADDRESS
SECOND LINE	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	
THIRD LINE	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	
FOURTH LINE	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	

4x20 DMM, 1/16 MUX N=1 : 2-LINE DISPLAY F=0 : 5X7 DOTS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
																					DISPLAY POSITION
FIRST LINE	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	DD RAM ADDRESS
SECOND LINE	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	
THIRD LINE	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	
FOURTH LINE	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67	